REMARKS/ARGUMENTS

This Amendment is in response to the Office Action dated May 5, 2006. Claims 1-45 are pending in the present application. Claims 1-23 and 34-45 have been previously canceled in a Preliminary Amendment filed on August 28, 2003. Claims 24-33 have been rejected. Claim 24-33 have been amended to further define the scope and novelty of the present invention, to address §101 and §112 rejections, and to correct typographical and grammatical errors, in view of the Examiner's comments, in order to place the claims in condition for allowance. Support for the amendments to the claims is found throughout the specification, and in particular, in Figure 7; on page 5, lines 13-17; on page 11, lines 14-23; on page 20, lines 8-19; on page 23, lines 7-16; and on page 27, lines 14-23. Applicants respectfully submit that no new matter has been presented. Claims 24-33 remain pending. For the reasons set forth more fully below, Applicants respectfully submit that the claims as presented are allowable. Consequently, reconsideration, allowance, and passage to issue are respectfully requested.

Claim Rejections - 35 U.S.C. §101

The Examiner has stated:

> **Claim 24 is rejected under 35 U.S.C. 101 because the claimed invention is non-functional descriptive material, abstract idea, and no tangible result. The steps in the claimed invention are non-relationship or linking together. They are also lacking the step of how a full match for a variable length search key to be searched/occurred. The final result is not tangible...**

In response, claim 24 has been amended to address the above-referenced rejection. Specifically, claim 24 has been amended to more clearly interrelate the elements and to more clearly recite the matching function. Applicants respectfully submit that claim 24, as amended, now complies with 35 U.S.C. §101.

Support for the amendments to the claim is found throughout the specification, and in particular, in Figure 7; on page 5, lines 13-17; on page 11, lines 14-23; on page 20, lines 8-19; on page 23, lines 7-16; and on page 27, lines 14-23.

Claim Rejections - 35 U.S.C. §112

The Examiner has stated:

> **Claim 24 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted element is: how the process of determining a full match for a variable length search key is. The body of the claim 1 does not include/prove/perform what set forth in the preamble of the claim. The body of the claim 1 does not have the process of determining a full match for a variable length search key and what the search key is.**

In response, as described above with respect to the 35 U.S.C. §101 rejection, claim 24 has been amended to address the above-referenced rejection. Specifically, claim 24 has been amended to more clearly interrelate the elements and to more clearly recite the matching function. Applicants respectfully submit that claim 24, as amended, now complies with 35 U.S.C. §112, second paragraph.

Claim Rejections - 35 U.S.C. §102

The Examiner has stated:

> **Claims 24-33 are rejected under 35 U.S.C. 102(b) as being based upon a public use or sale of the invention. Patent No.: US 6,404,752 B1 issued to Allen, Jr. et al. (hereinafter Allen).**
>
> **With respect to claim 24, Allen teaches an apparatus fabricated on a semiconductor substrate for determining a full match for a variable length search key (a switch network apparatus having components, control point processor, interface device, very large scale integrated (VLSI) circuit device or chip which as a semiconductor substrate, together being formed a network processor with tree search algorithm for determining variable length key matches: abstract, col. 5, lines 60-67 col. 6, lines 1-22, col. 7, lines 55-67 and col. 8, lines 1-22), comprising:**

an embedded processor complex including a plurality of protocol processors and an internal control point processor that provide frame processing (protocol processors or network and control point processors that for performing data frame processing such as parsing and translation or transformation protocol: col. 4, lines 32-55);

a plurality of hardware accelerator co-processors accessible lo each protocol processor and providing high speed pattern searching, data manipulation, and frame parsing (performing pattern searching based on the data frames that are dispatched to the next available protocol processor for performing frame lookups (col. 7, lines 55-67 and col. 8, lines 1-22);

a plurality of programmable memory devices that store a plurality of data structures that represent at least one search tree, wherein the data structures include a direct table, a pattern search control block and a leaf (a plurality of programmable device memory to store data structures: col. 5, lines 54-58 and col. 24, lines 22-35; see figs. 14 & 15: data structure with direct table with leaf, pattern search control block (PSCB): col. 25, lines 48-67); and

an control memory arbiter that controls the access of each protocol processor to the plurality of memory devices (memory devices: see fig. 1, 12 and 13, col. 7, lines 15-38). ...

Applicants respectfully traverse the Examiner's rejections. The present invention provides an apparatus fabricated on a semiconductor substrate. In accordance with the present invention, the apparatus includes an embedded processor complex including a plurality of protocol processors and an internal control point processor that provides frame processing. The apparatus also includes a plurality of hardware accelerator co-processors coupled to the embedded processor complex. The plurality of hardware accelerator co-processors are accessible to each protocol processor and provide high speed pattern searching, data manipulation, and frame parsing. The apparatus also includes a plurality of memory devices coupled to the embedded processor complex. The plurality of memory devices store a plurality of data structures that represent at least one search tree. The data structures include a table having entries, where at least one entry stores a leaf, and where the at least one leaf includes a pattern corresponding to a search key containing an address. The apparatus also includes a control memory arbiter coupled to the plurality of protocol processors. The control memory arbiter controls the access of each protocol processor to the plurality of memory devices, and the table

stored in the plurality of memory devices is utilized to match the pattern with the search key. Allen does not teach or suggest these features, as discussed below.

Allen discloses a network switch using a network processor and methods. The network switch includes interface processors and peripherals that together form a network processor capable of cooperating with other elements including an optional switching fabric device in executing instructions directing the flow of data in a network. (Abstract.)

However, Allen does not teach or suggest the "plurality of hardware accelerator co-processors coupled to the embedded processor complex, wherein the plurality of hardware accelerator co-processors are accessible to each protocol processor and provide high speed pattern searching, data manipulation, and frame parsing," as recited in amended independent claim 24. The Examiner has referred to a function of performing pattern searching based on data frames as being the same as the "plurality of hardware accelerator co-processors" of the present invention, referring to column 7, lines 55-67, and to column 8, lines 1-22 of Allen. However, these sections do not mention hardware accelerator co-processors. In fact, nowhere does Allen teach or suggest hardware accelerator co-processors as in the present invention.

Furthermore, Allen does not teach or suggest the "plurality of memory devices store a plurality of data structures that represent at least one search tree, wherein the data structures include a table comprising a plurality of entries, where at least one entry stores a leaf," as recited in amended independent claim 24. Instead, Allen teaches a direct table having entries that **point to** leaves (Figure 15B of Allen). In contrast to the direct table of Allen, referring Figure 7 of the present invention, the table of the present invention includes entries that "have leaves stored in them" (specification, page 27, lines 14-23).

Therefore, Allen does not teach or suggest the cooperation of elements as recited in amended independent claim 24, and claim 24 is thus allowable over Allen.

Dependent claims

Dependent claims 25-33 depend from amended independent claim 24. Accordingly, the above-articulated arguments related to amended independent claim 24 apply with equal force to claims 25-33, which are thus allowable over the cited reference for at least the same reasons as claim 24.

Conclusion

In view of the foregoing, Applicants submit that claims 24-33 are patentable over the cited reference. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicants' attorney believes that this application is in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call Applicants' attorney at the telephone number indicated below.

Respectfully submitted,
SAWYER LAW GROUP LLP

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Date

Joseph A. Sawyer, Jr.
Attorney for Applicant(s)
Reg. No. 30,801
(650) 493-4540